ON-WAFER LARGE SIGNAL PULSED MEASUREMENTS

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INTRODUCTION

Sophisticated design tools are now available for non-linear microwave circuit design.

Many simulators have been developped and give reliable results.

However, sometimes, predicted results differ from the experimental ones ; the difference is generally due to a bad modeling of the active devices used.

An important step in the design of non-linear MMICS is then an accurate largesignal characterization and modeling of the semi-conductor devices |1| |2| |3| |4|.

We present in this paper an on-wafer fully-automated pulsed-measurement system allowing to extract automatically the characteristics of the non-linear current generators of a FET in function of the gate to source (Vgs) and drain to source (Vds) voltages.

These sources are :
- the drain current generator: Ids = f(Vgs, Vds)
- the gate-schottky diode generator : Igs = f(Vgs)
- the gate-drain avalanche generator : Igd = f(Vgs, Vds).

The measurement-system is coupled to a data-processing software which includes a fitting algorithm. The fitted equation is then displayed as output data and may be transferred to a non-linear simulator, such as a spectral balance simulator described else where |5|.

Measurements may be performed at different temperatures, pulse-widths and duty-cycles, in view of modeling the trapping and temperature effects |6|.

I - PRINCIPLE OF OPERATION

Figure 1 shows the pulse measurement setup : all the test instruments have either IEEE 488 or HP IL Bus capability.

A desktop computer is used for control, data acquisition and data processing.

The measurement-system proceeds as follows :
* A fast rise-time pulse voltage is applied to the gate of the FET under test.
* The gate-voltage generator triggers a low level drain pulse generator with a time delay which may be up to 50 ns.
This voltage generator drives a power pulse generator, which delivers a power pulse to the drain of the FET.
* Both gate and drain pulses are applied to the FET throught waferprobes, via microwave absorbers, to eliminate possible oscillations at microwave frequencies.
* Resulting FET current is displayed, with the drain and gate voltages to a digitized oscil loscope. 500 measurements are averaged for every measured point.

II - DRAIN POWER PULSE GENERATOR CHARACTERISTICS

To measure accurately the FET non-linearities, the resulting pulse current must not be distorted. But it is well known that the FET drain-port may present a highly variable impedance following the applied voltages.

So, the drain generator must be able to support those impedance variations, for low-level or high-power FETS.

The maximum amplitude of the current/voltage pulse that may be delivered to the drain is 3 amperes/40 volts.

Pulse duration may vary from 200 ns to 1 ms. Pulse repetition rate may be increased from 600 ns to 1 ms.

Finally the drain and gate pulse generators may deliver a Dc offset voltage without altering the pulse voltage. So the pulse measurements may be made at any desired Dc bias.

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III - MEASUREMENT PROCEDURE AND DATE PROCESSING

The system measures the external currents Id and Ig in function of the external voltages VG and VD as indicated in figure 7.

The users is asked on the maximum values which must not be exceedeed by Vg and Vd voltages : figure 2.

At frequencies under consideration: Cds and Cgd are open circuits and the inductances Lg, Ld, Ls may be neglected (the more the transistors are measured on-wafer). Once the resistances of the FET have been determined by DC measurements, the following equations must be solved to find the internal current generators of the FET : Ids, Igs, Idg in function of the internal voltages Vds and Vgs.

$$V_G = V_{gs} + I_G (R_g + R_i + R_s) + I_D . R_s \quad (1)$$

$$V_D = V_{ds} + I_D (R_d + R_s) + I_G . R_s \quad (2)$$

where : $I_D = I_{ds} + I_{dg}$

$I_G = I_{gs} - I_{dg}$

IV - RESULTS OBTAINED

To demonstrate the validity of the measurements figures 3 and 4 show an example of the pulse-shapes of Id, Vd.

Figures 5 shows the resulting of pulsed measurements of a FET.

Note that the curves have not been smoothed.

Finally, figure 6 shows, for a given FET, an example of the resulting analytical curves, fitted with equations of the reference | 7 |.

The figure 7 indicates the resulting non-linear FET model with the corresponding numerical values.

V - IMPROVEMENTS OF THE NON-LINEAR MODELING

Modeling the non-linear current-sources by analytical formulas or polynomial approximations gives good results at high levels ; however these formulas are technologie dependent, moreover there are still problems with the small signal transconductance and drain conductance derived from the analytical formulas. To improve the non-linear modeling at low and high level a new procedure is under development which uses tensor product splines, in place of analytical formulas.

This technique, which is technology independent, includes a fit-strategy which minimizes not only the current deviation in every point but also the slope deviation.

CONCLUSION

A fully automated on-wafer pulsed measurement set-up is presented. It allows accurate measurements and modeling of non-linear current-sources of FETS.

A signifiant feature of the system is that it measures automatically the non-linear characteristics of FETS minimizing time and effort involved in measuring devices.

Moreover measurements performed for different DC and pulse widths voltages conditions allow to extract accurate nonlinear FET models and analyze the trapping and temperature effects.

The three key "components" of the system are :

* the power-pulse generator which delivers drain pulses without distortion

* the microwave absorbers which eliminate the possible high-frequency oscillations

* the associated software programmed in Pascal language, which controls the instruments, processes a high number of data, fitts the measured data to analytical expressions, and finally displays the results as :
  - data file
  - or current curves in function of V_{gs} and V_{ds}.

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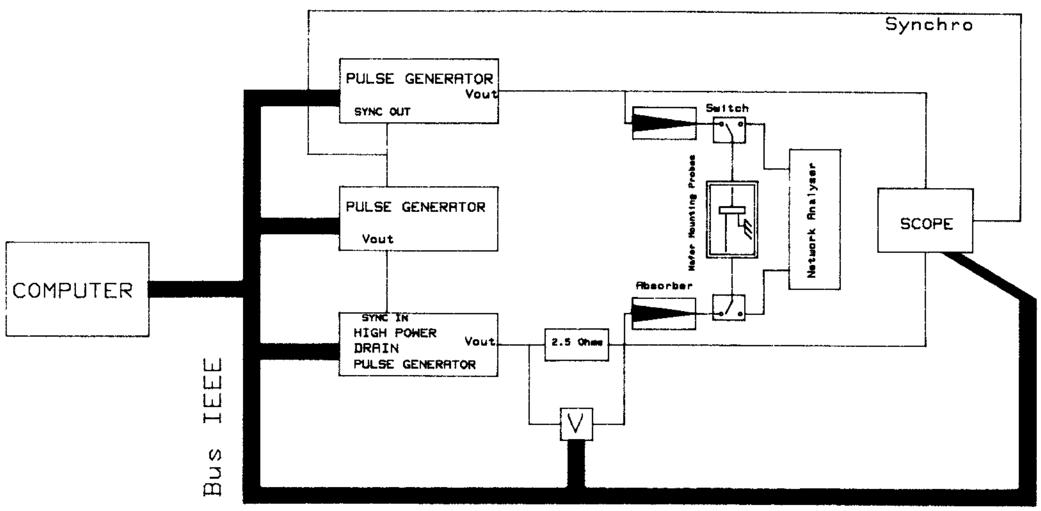


Fig. 1 : Pulse measurement set-up

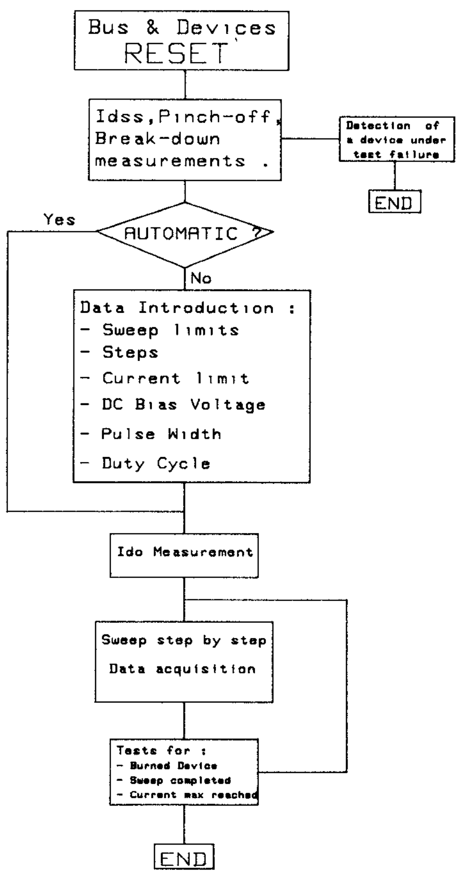


Fig. 2 : Measurement procedure

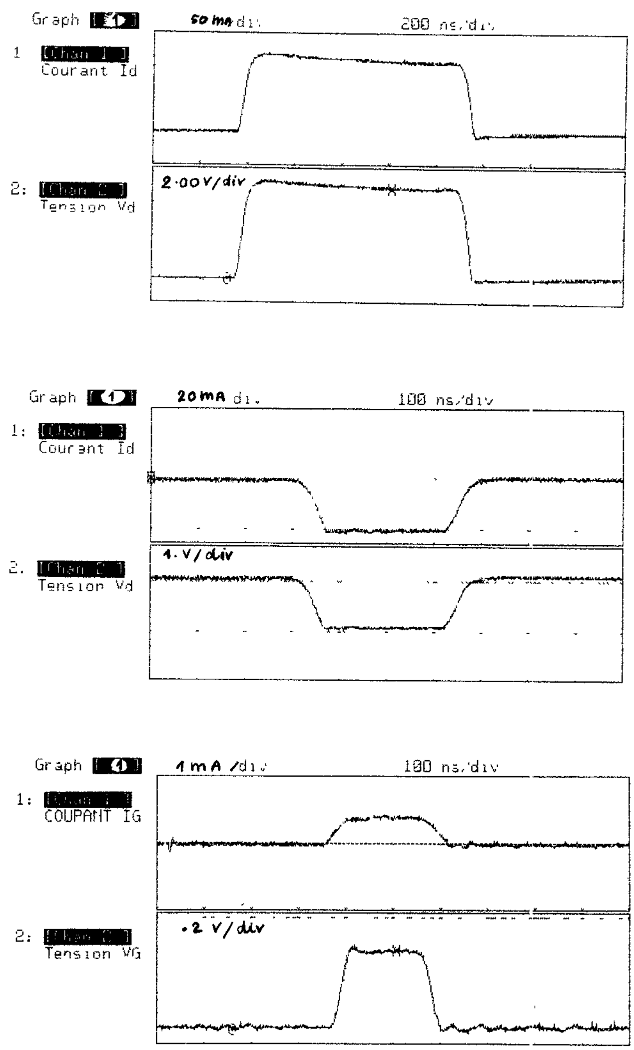
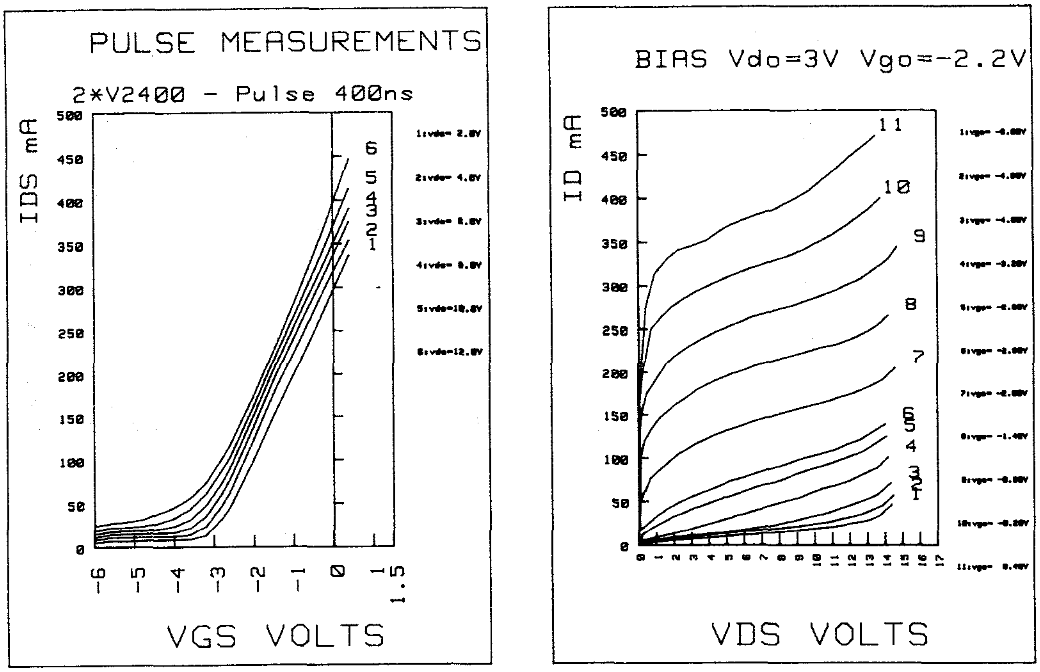


Fig. 3 and 4 : Drain and voltage pulse sharpes

Fig. 5 : Results obtained with a : 2 * V2400 Thomson transistor



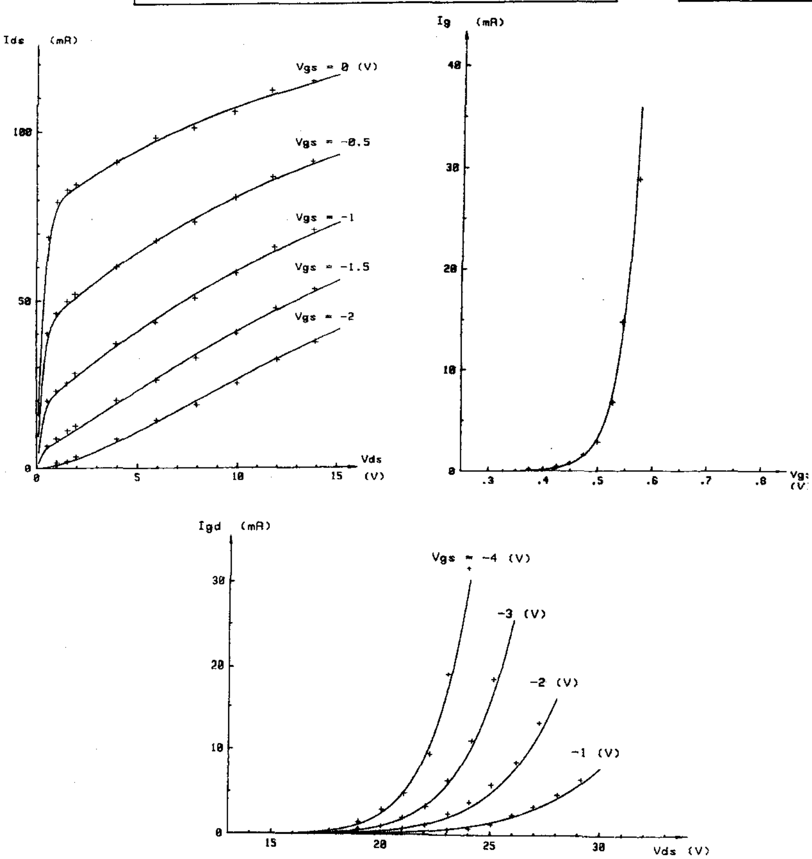
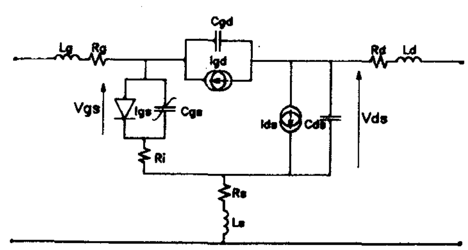


Fig. 6 : Comparison between fitted and measured points



Rg = 1.22ohm	Rd = 0.6ohm	Rs = 0.6ohm
Lg = 0.153nH	Ld = 0.197nH	Ls = 0.0329nH
Ri = 2.5ohm	τ = 6.0pS	
Cds = 0.123pF	Cgd = 0.0433pF	

Ids: Idss = 164.2mA m = −0.831 a = 0.124 b = 0.02316 p = 0.2182
Vpo = 2.038 Vdsp = 0.3951 w = 0.7367 Vphi = 0.853

Igd: Io = 322.657nA a = −0.7642 b = 0.0619 c = 5.0131 d = 0.8181
e = 1.3657

Ig: Is = 1.0nA α = 30.0

Cgs: Cgso = 0.9437pF V_ϕ = 0.8V

Fig. 7: Resulting non-linear analytical FET model